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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,069	11/19/2003	Steven H. Voldman	BUR920030096US1	1068

29625 7590 10/12/2005

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EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,069	VOLDMAN, STEVEN H.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *15-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 27* is/are rejected.

7)☒ Claim(s) *9-14* is/are objected to.

8)☒ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/19/2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/19/03 and 11/24*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-14; and 27 (Group I), drawn to a method modification placement for optimizing latchup of an integrated circuit based on element density, classified in class 716, subclass 9.

II. Claims 15-20 (Group II), drawn to a method placement for optimizing latchup of an integrated circuit based on element density, classified in class 716, subclass 10.

III. Claims 21-23 (Group III), drawn to a method placement for optimizing latchup of an integrated circuit based on mathematical graph representation, classified in class 716, subclass 10.

IV. Claim 24 (Group IV), drawn to a method placement for optimizing latchup of an integrated circuit based on cost factor, classified in class 716, subclass 10.

V. Claims 25-26 (Group V), drawn to a method placement for optimizing latchup of an integrated circuit associated with gate/transistor level, classified in class 716, subclass 10.

2. Inventions Groups I, II, III, IV, and V are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group I has separate utility such as a method of modification placement for optimizing latchup of

an integrated circuit based on element density. Invention Group II has separate utility such as a method placement for optimizing latchup of an integrated circuit based on element density. Invention Group III has separate utility such as a method placement for optimizing latchup of an integrated circuit based on mathematical graph representation. Invention Group IV has separate utility such as a method placement for optimizing latchup of an integrated circuit based on cost factor. Invention Group V has separate utility such as a method placement for optimizing latchup of an integrated circuit associated with gate/transistor level. See MPEP § 806.05(d).

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, and the search required for Group I is not required for Group II, III, IV, and V; the search required for Group II is not required for Group I, III, IV, and V; as same as Group III, Group IV and Group V, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with the Applicant's attorney Mr. Richard Kotulak (Reg. No. 27712) on September 15th, 2005 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-14 and 27. Affirmation of this election must be made by applicant in replying to this Office action. Group II, claims 15-20; Group III, claims 21-23; Group IV, claim 24; and Group V, claim 25-26 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention. The Applicant's are requested to cancel claims 15-26 in the next office communication.

5. In this Office Action, Group I, claims 1-14 and 17 are going to be examination.

Claim Objections

6. Claims 1-14 and 27 are objected to because of the following informalities: the claim preamble must state the intended use or purpose of the invention. New preambles are suggested:

As per claim 1 -- a method of optimizing latchup for an integrated circuit --.

As per claim 27 -- a computer program product of optimizing latchup for an integrated circuit --.

As per claim 10 contains terms "BP" and "ROX", clarified and spell out these terms in the claim.

Claims 12-14 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

As claim 12 recited the limitation that "a relative distance between a location of an injecting source and collecting circuit ". This limitation has not been recited in claims 1 and 9, which is claim 12 depending on.

As claim 13 recited the limitation that "an injection current strength". This limitation has not been recited in claims 1, 9, and 12, which is claim 13 depending on.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. **Claims 1, 5 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Guruswamy et al. (Guruswamy) (US 5,901,065).**

9. **With respect to claims 1 and 27**, Guruswamy disclose a method and computer program product (abstract) comprising the steps of:

(as claim 27) a computer usable medium having computer readable program code (instructions) embodied in the medium (fig, 7; col. 12, ll. 23-67), the computer program product having:

(as claims 1 and 27) (computer program for) identifying (estimating) element density of at least one functional circuit block (col. 8, ll. 65-67 and col. 9, ll. 1-3);

(as claims 1 and 27) (computer program for) identifying element attributes of elements associated with the at least one functional circuit block (col. 9, ll. 4-17 – the first transistor (element) relative attribute to adjacent transistor (element)--);

(as claims 1 and 27) (computer program for) forming an element density function parameterized (space distance interval is scaled by a factor) from the element attributes (col. 7, ll. 19-23 and col. 9, ll. 54-67, -- determined the element locations, dimensions, and space rule, which are associated with element density function parameterized --) ; and

(as claims 1 and 27) (computer program for) modifying (adjusted) placement of the at least one functional circuit block relative to other functional circuit blocks based on the element density function to substantially (col. 9, ll. 48-59) eliminate latching effects in a circuit (col. 12, ll. 43-53).

10. **With respect to claim 5**, Guruswamy disclose the method of claim 1, further comprising providing decoupling capacitor elements to fill space or add capacitance to eliminate propagation adjacent an injection source to avoid propagation of latchup or soft latchup (col. 9, ll. 24-32 – prevent unwanted conduction or crosstalk--).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 2-4, 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guruswamy et al. (Guruswamy) (US 5,901,065) in view of Ker et al. (Ker) (Layout design and verification for cell library to improve ESD/Latchup reliability in Deep-Submicron CMOS technology, *IEEE 1998 Custom Integrated circuit conference).*

13. **With respect to claims 2-4 and 6-8**, Guruswamy disclose all the limitations of claim 1 as rejection 35 USC 102 above.

Guruswamy does not explicitly teach (claims 2-4 and 6-8) placing the NFET and PFET density associated with element density. Undershoot and overshoot, which are included identifying element attribute and spacing.

Ker teach a method of (claims 3 and 6) improved latchup by placing the NFET and PFET density of a given function circuit block away from the source of undershoot and overshoot, respectively. (at least suggest at fig. 9 (b), -- reduce a contact area for improved latchup, and modifying layout associated with distance between ESD element and adjacent region of high pnpn density--) and (as claim 2) NFET and PFET density is associated with element density (at least suggest at figures 10 (worst) and (good). Moreover, (claim 3-4, and 7-8) figure 10 (good) give the best solution to move function circuit block away from the source of undershoot and overshoot which is identifying element relative attribute spacing of one function block to the other.

It would have been obvious to one of ordinary skill in the art at the time invention was made would combine Guruswamy and Ker references for improved the latchup of scaled down or compacted an IC in circuit design by modification a placement (layout) associated with space density and latchup characterizes functions.

Allowable Subject Matter

14. Claims 9-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. The following is a statement of reasons for the indication of allowable subject matter:

As per claim 9, the prior art fails to teach the limitation "a step of determining magnitude of latchup sensitivity of a specific circuit by":

$$F=\beta_{npn}\beta_{pnp}/[(I_{DD}+I_{RW}\beta_{npn})/(I_{DD}-I_{RW}-I_{RS}(\beta_{npn}{}^{+1})/(\beta_{npn}))]$$

As per claim 10, the prior art fails to teach the limitation "counting of independent ROX shapes indicating the number of npn elements associated with the at least one functional circuit block".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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